REMARKS

This is intended as a full and complete response to the Office Action dated May 20, 2004 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on August 20, 2004. Claims 1-24 are presently pending in the above-captioned application.

Reconsideration of the application in view of the enumerated amendments and the following remarks is respectfully requested.

Rejection of Claims 17-20

Claims 17-20 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, objection is made in the Office Action to the fact that claim 17, a method claim, refers to claim 15, a product claim. Claims 18 - 20 were rejected as depending from claim 17.

Claim 17 is currently amended to reflect its dependency from claim 16, a method claim. This merely corrects a minor inadvertent clerical error, and thus does not relate to prior art. Accordingly, it is respectfully submitted that the ground of rejection of claim 17 is overcome. As claims 18-20 depend, either directly or indirectly, from claim 17, it is likewise submitted that the ground of rejection of claims 18-20 is overcome for like reasons. Accordingly, Applicant respectfully requests that the above-identified rejection of claims 17-20 be withdrawn.

Rejection of Claims 1-19

Claims 1-19 were rejected under 35 U.S.C. 102(b) as being anticipated by Eisenmann et al. "Power Calculation for High Density CMOS Gate Array's," IEEE Euro ASIC '91, pp. 198-203 (May 1991), (hereinafter, "Eisenmann"). With respect to the rejection of claims 1-9 and 16-20, Applicant has amended claims 1 and 16, respectively. With respect to the rejection of claims 10-15, Applicant respectfully disagrees.

Claims 1-9

Eisenmann at column 2 of page 201, states that "[t]o calculate the power requirements of a design it has to be simulated with a sequence of application patterns which generate the most activity." In that same paragraph, Eisenmann goes on to state that "[t]hese patterns can also occur within a normal simulation…" and "[i]n that case the start- and end-times for the event count have to be specified correctly because only average frequencies are calculated with this method."

In contrast to Eisenmann, claim 1 as amended recites in relevant part: "…dividing the activity factor by sampling time, which is a fraction of simulation time, to obtain the frequency…" In other words, the invention as claimed in claim 1 does not determine an overall average frequency for an entire simulation run for determining dynamic power dissipation. Rather, frequency is determined from sampling time. This is a nontrivial distinction because a node, and thus a circuit associated therewith, may be more or less active depending on simulation stimulus, and thus dynamic power consumption may vary with sampling periods within a simulation interval depending on which circuits are or are not active.

Accordingly, it is respectfully submitted that claim 1 as amended is not shown or described by Eisenmann, and thus Applicant respectfully requests that the rejection of claim 1 be withdrawn. Moreover, claims 2-9 which directly or indirectly depend from allowable base claim 1 are likewise allowable.

Claims 10-15

In the Office Action, it is stated that Eisenmann's POWCAL "module produces a 'macro power file' corresponding to the testbench of claim 14 and also produces a 'report file' corresponding to the power dissipation code of claim 15." With this characterization of Eisenmann, Applicant

respectfully and completely disagrees. In Eisenmann at column 1 of page 199, it is stated that a "delay calculator" ("DECAL™") and a "logical simulator" ("VERILOG®") work as preprocessors to a power calculator ("POWCAL").

Eisenmann at column 1 of page 201 states that an "…event driven logical simulator VERILOG® can be used to measure times and events." These events and times may be used to determine toggle frequency. In that same paragraph on Page 201, Eisenmann goes on to state that an "…event-count-function counts the number of events on a specified target while a given trigger condition is true… and the time-count-function measures the time while the specified target is true." Continuing in the same paragraph on Page 201, Eisenmann states that "[s]pecial power calculation sections were built in the verilog models with these functions by stating a function for every probe point (target) of interest." Thus, Eisenmann builds in each Verilog model power calculation sections with event-count functions and time-count functions. This is further borne out in Eisenmann at column 1 of page 203, where it is stated that "[t]he system is not based on estimations or statistics, but on simulations of the circuit in a real application and on a pre-characterized power library."

Furthermore, in column 1 on page 202 of Eisenmann it is stated that POWCAL uses formulas (2) to (6) to create "two report files, the powcal-report-file and the macro-power-file." Eisenmann in that same paragraph goes on to state what is in the respective files:

> "The report file contains the total power consumption of the circuit and a detailed listing of all power components. The macro power file provides a list of all instances and their power dissipation."

First, both the report file and the macro power file in Eisenmann are data outputs of a system. In contrast, power dissipation code is code, and a testbench is both code and an

input. A "testbench" is code written to provide stimulus to a device under test, and it may be employed to simulate application of signals to a simulated integrated circuit.

Secondly, Eisenmann pre-characterizes libraries with functions to measure times and events to provide a toggle frequency. In other words, a limitation of Eisenmann is that the power calculation sections are built into the Verilog model. In contrast, power dissipation code is code used to annotate a model. Model annotation is done after creation of the model, and not code built into the model as in Eisenmann. Advantageously, such power dissipation code may be subsequently used on another model.

For the above-mentioned reasons, it should be understood that Eisenmann is completely silent on generating power dissipation code, as claimed in claim 10, and annotating a model, as claimed in claim 15, or a testbench, as claimed in claim 14 using the power dissipation code generated. Accordingly, it is respectfully submitted that Eisenmann does not show or describe claims 10, 14 and 15, as originally presented, and thus Applicant respectfully requests that the rejection of those claims be withdrawn. Moreover, claims 11-13, which directly or indirectly depend from allowable base claim 10, are likewise allowable, and thus Applicant respectfully requests that the rejection of those claims be withdrawn.

Claims 16-20

In the Office Action, claim 20 was indicated as having allowable subject matter. Claim 20 has been canceled without prejudice to amend claim 16. Claim 16 has been amended with the subject matter previously claimed in claim 20. Accordingly, it is respectfully submitted that claim 16, and claims 17-19, which directly or indirectly depend from claim 16, are in condition for allowance, and thus Applicant respectfully requests that the rejection of claims 16-19 be withdrawn.

Allowable Subject Matter

In the Office Action, it was indicated that claims 21-24 are allowed.

CONCLUSION

All claims should now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the undersigned can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

Justin Liu
Attorney for Applicant
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 12, 2004.

Julie Matthews
Name

Signature